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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/717,284 | 11/19/2003 | Robert C. Taft | 08211/0200252-US0 | 7398 |
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| DARBY & DARBY P.C. P.O. BOX 5257 NEW YORK, NY 10150-5257 | | | | NGUYEN, HIEP |
| ART UNIT | | PAPER NUMBER | | |
| | | 2816 | | |

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|------------------------------|------------------------|---------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/717,284 | TAFT ET AL. |
| | Examiner | Art Unit |
| | Hiep Nguyen | 2816 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 11-19-03.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

| | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>10-19-04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and / or clarification is required.

Regarding claim 1, the recitation “a constant-voltage boosting circuit for maintaining substantially constantly the control voltage at a substantially constant value above a voltage of the input signal” is indefinite because it is misdescriptive.

Figure 8 of the present application shows that the input signal (Vin) is also connected to the constant-voltage boosting circuit (820). Thus, the control voltage (Vgn) is not constant because it is controlled by the levels of the input voltage. The same rationale is applied to claims 14, 17 and 18.

Regarding claims 4 and 16, the recitation “wherein the constant-voltage boosting circuit includes a component exhibiting a characteristic voltage behavior” is indefinite because it is not clear what is the meaning of “a component exhibiting a characteristic voltage behavior” is. Every component of an electronic circuit exhibits a characteristic voltage behavior (diode, transistor etc.)

Regarding claim 6, the recitation “the component includes a junction between two dissimilar materials” is indefinite because it is not clear what it is meant by. The Applicant is requested to point out this component in the drawing.

Regarding claims 7 and 20, the recitation “and a component exhibiting a characteristic voltage difference” is indefinite because it is not clear what the “a characteristic voltage difference” is meant by.

Regarding claim 9, the recitation “the transmission switch exhibits a characteristic behavior that changes depending on a value of an input signal”: is indefinite because it not clear what kind of “characteristic behavior” the transmission switch has. According to figure 3 of the present application, the transmission switch

passes the input signal when activated by the control signal. There is no “characteristic behavior that changes depending on a value of an input signal” seen. The Applicant is requested to show in which drawing claim 9 reads on.

Regarding claim 10, the recitation “the characteristic behavior is that a threshold voltage of the main NMOS transistor changes depending on the input signal value” is indefinite because it is misdescriptive. The threshold voltage (V_{gs}) of the main NMOS (310) in figure 3 is independent of the input signal. Claim 10 is also indefinite because it is not clear how the “a behavior of a threshold voltage of the control NMOS transistor” can substantially cancel the “characteristic behavior”. The Applicant is requested to clarify what the “a characteristic behavior”, “a behavior of a threshold voltage of the control NMOS transistor” are meant by. The Applicant is also requested to point out what is the “a control NMOS transistor” in the drawing.

Regarding claim 12, the recitation “a calibration transmission gate coupled to the output node, and having an input node coupled to receive a calibration signal associated with the input voltage” is indefinite because it is not clear what “associated with the input voltage” is meant by. Figure 10 of the present application shows that the calibration transmission gate (610) receives a calibration signal (V_{cal}) that is different (not associated) from the input signal (V_{in}). The Applicant is requested to show what drawing the circuit of claim 12 reads on.

Regarding claim 17, the recitation “means for applying the control voltage to control the generation of the output voltage” is indefinite because no such “means” is seen. The control voltage is applied directly to the gate of the switch. The Applicant is requested to point out the “means” in the drawing.

Claims 2, 3, 5, 8, 11, 13, 15, and 19 are indefinite because of the technical deficiencies of claims 1, 14 and 18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 and 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kanda et al. (US Pat (6,469,573)).

Regarding claims 1, 2 and 3, figures 8 and 9 of Kanda shows a transmission circuit comprising:

- an input node (PAD2) for receiving an input signal;
- an output node for generating thereon an output signal from the input signal;
- a transmission switch (QN2) coupled between the input node and the output node, the transmission switch having a control terminal and being controlled by a control voltage at the control terminal; and

a constant-voltage boosting circuit (241) for maintaining substantially constantly the control voltage at a substantially constant value above a voltage of the input signal (col. 11, lines 1-6). It is inherent that when the transmission gate is turned off, there is no current flowing through it and when it is turned on, the input signal is transmitted to the output of the transmission gate. The constant-voltage boosting circuit (241) is coupled between the input node and the control terminal. Note that the supply voltage (Vextpw) is applied to (PAD2) (col. 9, lines 11-21). Thus the control voltage (V_{bt}) = $V_{extpw} + 2 V_{th} = \text{constant}$.

Regarding claims 4, 5 and 6, figure 9 of Kanda shows that the constant-voltage boosting circuit comprises diodes (DN16, QN17), components exhibiting a characteristic voltage behavior) and MOS transistors (QN11-QN13). The diodes comprise two dissimilar materials and the voltage drop is developed at a junction connecting the two dissimilar materials (anode-cathode).

Regarding claims 7 and 8, the current source is transistor (QN13) and the “and a component exhibiting a characteristic voltage difference” is diode (QN14). The preboosting circuit comprises elements (I3) and (C11). Elements (QN14, QN15) are coupled between the preboosting node and the control terminal.

Regarding claim 9, the transmission switch exhibits “a characteristic behavior” that changes depending on a value of the control signal (V_{bt}), and the

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constant-voltage boosting circuit maintains the control voltage at a value above ($V_{in} + 2V_{th}$, col. 11, lines 1-6) the control signal voltage that is further adjusted (boosted) so as to substantially compensate for the “characteristic behavior” of the transmission switch. The high control voltage increases (adjusts) the speed of the transmission switch due to high control voltage (see US Pat. 4,404,237, col. 2, lines 54-58).

Regarding claims 10 and 11, switch (QN2) is an NMOS transistor. The constant-voltage boosting circuit (figure 9) includes “a control NMOS transistor” (Q16 or Q17). The voltage (V_{th}) drop across transistor (Q16) or (Q17) regulates voltage (V_{bt}). The high voltage (V_{bt}) “cancels the characteristic behavior” of the transmission switch (QN2) by turning it on more strongly to speed up the passage of the signal. The PMOS transistor (QN14) has a gate coupled to the input signal (V_{in}).

Regarding claim 13 the second transmission switch (QN3) is coupled to the input node (PAD2) and a second output node (Vextref).

Regarding claims 14-16, figures 8 and 9 of Kanda show a transmission gate for generating an output signal from an input signal comprising:

a switch (QN2) including a gate terminal adapted to receive a control voltage (V_{bt}), and a source terminal and a drain terminal, wherein one of the source terminal and the drain terminal is adapted to receive the input signal (V_{in}), and the other one of the source terminal and the drain terminal is adapted to provide the output signal thereon; and

a constant-voltage boosting circuit (241) to generate the control voltage having substantially constantly a voltage with a substantially constant value ($V_{extpw} + 2V_{th}$) that above a voltage of the input signal (V_{extpw}). The constant-voltage boosting circuit receives the input signal (V_{in}). The voltage boosting circuit comprises diodes (DN16, QN17) that are components exhibiting a characteristic voltage behavior).

Regarding claim 17, figures 8 and 9 of Kanda show a device comprising:

means for receiving an input voltage (PAD2);

means for generating an output voltage (QN2) from the input voltage;

means for regulating a preboosted voltage (241) to generate a control voltage (V_{bt}) having substantially constantly a substantially constant value above the

input voltage; and “means for applying the control voltage” (the gate of QN2) to control the generation of the output voltage.

Regarding claim 18, figures 8 and 9 of Kanda shows a method comprising:

receiving an input voltage and generating an output voltage (QN2) ;

regulating a preboosted voltage (elements QN16, QN17) to generate a constant control voltage (Vbt);

applying the control voltage to switch (QN2) to generate the output voltage.

Regarding claim 19, the method of claim 18, further comprising:

pumping charge at a preboosting node to generate the preboosted voltage (Fig. 9).

Regarding claim 20, regulating is performed by passing a bias current through a component exhibiting “a characteristic voltage difference” (diodes QN16, QN17).

Claims 1-10, 12 and 14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Mathew et al. (US Pat. 6,404,237).

Regarding claims 1-3, figure 2A of Mathew shows a transmission circuit comprising:

input, output nodes;

a transmission switch (290, 230);

a constant boosting circuit (212, 232, 236, 238) generating a voltage ($V_{cc}+dv$) higher than the input voltage. Note that the input voltage (IN) cannot be higher than the supply voltage (V_{cc}). It is inherent that when the transmission switch is turned off, no current will flow through it and when the transmission switch is turned on, the switch will pass the signal through (high integrity).

Regarding claims 4 and 5, capacitor (234) exhibits a characteristic voltage behavior (voltage boosting). The MOS transistor is (236).

Regarding claims 6-8, MOS transistor (236) includes “a junction between two dissimilar materials” i.e., gate, dielectric and substrate and there is a voltage

difference between that gate and the substrate. Current source (232) drives a current through the component. The preboosting circuit is capacitor (234) and inverter (212).

Regarding claim 9, “the transmission switch exhibits a characteristic behavior” that changes depending on a value of the control signal, and the constant-voltage boosting circuit maintains the control voltage at a value above ($V_{cc} + dV$) the control signal voltage that is further adjusted (boosted) so as to substantially compensate for the “characteristic behavior of the transmission switch”. The high control voltage increases (adjusts) the speed of the transmission switch due to high control voltage (see US Pat. 6,404,237, col. 2, lines 54-58).

Regarding claim 10, because of the high level (behavior) of the control signal, the transmission switch is turned on faster i.e., “the characteristic behavior” (slow switching) is cancelled.

Regarding claim 12, figure 2A of Mathew shows a calibration circuit (290) having an input coupled to receive a calibration signal.

Regarding claims 14-16, figure 2A of Mathew shows a transmission gate comprising: a switch (230), receiving a control signal at the gate, having input/output terminal (IN/OUT), a constant -voltage boosting circuit (212, 234, 236, 238) generating a substantially constant voltage ($V_{cc}+dv$) that is higher than the input signal. Capacitor (234) exhibits a characteristic voltage behavior (harging/discharging behavior).

Regarding claim 17, figure 2A of Mathew shows a device comprising:

- means for receiving an input voltage (node IN);
- means for generating an output voltage (230) from the input voltage;
- means for regulating a preboosted voltage (236) to generate a control voltage having substantially constantly a substantially constant value above the input voltage; and means for applying the control voltage (the gate 230) to control the generation of the output voltage.

Regarding claim 18, figure 2A of Mathew shows a method comprising:

- receiving an input voltage and generating an output voltage;

regulating a preboosted voltage (236) to generate a constant control voltage ($V_{cc}+vd$);

applying the control voltage to switch (230) to generate the output voltage (OUT).

Regarding claim 19, the method of claim 18, further comprising:

pumping charge at a preboosting node (B) to generate the preboosted voltage;

Regarding claim 20, regulating is performed by passing a bias current through a component (transistor 236) exhibiting a characteristic voltage difference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

10-19-04



TUAN T. LAM
PRIMARY EXAMINER